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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
KIM, JUNG W	

ART UNIT	PAPER NUMBER
2132	

DATE MAILED: 09/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/982,042	FINDLING ET AL.	
	Examiner	Art Unit	
	Jung W. Kim	2132	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 October 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-16 are pending.

Information Disclosure Statement

2. The items listed on the Information Disclosure Statement filed on October 18, 2001 have been considered.

Drawings

3. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because the drawings are informal. All drawings must be made by a process which will give them satisfactory reproduction characteristics. Every line, number, and letter must be durable, clean, black (except for color drawings), sufficiently dense and dark, and uniformly thick and well-defined. The weight of all lines and letters must be heavy enough to permit adequate reproduction. This requirement applies to all lines however fine, to shading, and to lines representing cut surfaces in sectional views. Lines and strokes of different thicknesses may be used in the same drawing where different thicknesses have a different meaning. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings.

Claim Objections

4. Claim 1 is objected to because of the following informalities: replace "comprising the steps of;" with –comprising the steps of:--. The limitation "by shifting which of said bit locations includes said bit not set to said common state" does not properly identify which of the bits are shifted. Claim 13 is objected to because the claim is dependent to a method of claim 15; however, claim 15 recites a device. Claims 15 and 16 are objected to because the claims are dependent to a device of claims 1 and 2; however, claims 1 and 2 recite a method. Claim 14 is objected to because of the following informalities: the claim is not grammatical (see last limitation of the claim). Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mano et al. Logic and Computer Design Fundamentals, Chapter 5, "Registers and Counters" (hereinafter Mano) in view of Soenen et al. USPN 5,598,475 (hereinafter Soenen).

8. As per claim 1, Mano discloses a method of writing to a non-volatile memory including a total value incremented by a fixed amount (pgs. 261-263), the method comprising the steps of:

a. initializing a first memory location including multiple bits corresponding to specific bit locations such that all of the bits are set to a common state representing a first value (pg. 263, table 5-4, where Q3=0 and Q2=0);

b. initializing a second memory location including multiple bits corresponding to specific bit locations such that all of the bits except for one are set to a common state representing a second value (pg. 263, table 5-4, where Q1=0 and Q0=1);

c. combining the first and second values to obtain the total value (Q3 | Q2 | Q1 | Q0 represent the total value); and

d. increment the total value by a fixed amount by changing the second value of the second non-volatile memory location by shifting which of the bit locations includes the bit not set to the common state (next counting state is Q3=0, Q2=0, Q1=1, and Q0=0).

9. Mano does not disclose the first and second memory locations are non-volatile. Soenen discloses a non-volatile memory device for use in a rolling code security system, wherein a 40-bit security code is incremented when a transmission button is depressed and this incremented 40-bit security code is stored in non-volatile memory (col. 20:5-12). Storing the rolling code in non-volatile memory has the effect of retaining the code even when the power supply is shutdown, which is useful for retaining changing code values to remotely gain access to a secured perimeter. Therefore, it would be obvious to one of ordinary skill in the art the time the invention was made for the contents of the counters to be preserved in non-volatile memory, since it enables security systems to utilize a rolling code scheme for access to a secured perimeter, which is more secure than a stored static code security system (Soenen, 1:25-57). The aforementioned cover the limitations of claim 1.

10. As per claim 2, the rejection of claim 1 under 35 U.S.C. 103(a) is incorporated herein. (supra) In addition, the method further including the step of incrementing the total value by changing the first value of the first memory location by incrementing the one bit location in response to the second memory location being incremented through

all of the multiple bit locations (Mano, table 5-4; state: Q3=0, Q2=0, Q1=1, Q0=1, next state: Q3=0, Q2=1, Q1=0, Q0=0).

11. As per claim 3, the rejection of claim 2 under 35 U.S.C. 103(a) is incorporated herein. (supra) In addition, the step of incrementing the total value is further defined by combining a second value equal to one plus a maximum number of bit locations present in the second non-volatile memory location to the first value, and further including the step of setting the second value back to the initialized value (Mano, table 5-4; state: Q3=0, Q2=0, Q1=1, Q0=1, next state: Q3=0, Q2=1, Q1=0, Q0=0).

12. As per claim 4, the rejection of claim 1 under 35 U.S.C. 103(a) is incorporated herein. (supra) In addition, the bit not set to the common state in the second non-volatile memory location is a least significant bit (Mano, table 5-4; first state: Q3=0, Q2=0, Q1=0, Q0=1).

13. As per claim 5, the rejection of claim 1 under 35 U.S.C. 103(a) is incorporated herein. (supra) In addition, the bit not set to the common state in the second non-volatile memory location is a most significant bit (Mano, table 5-4; state: Q3=0, Q2=0, Q1=1, Q0=0).

14. As per claim 6, the rejection of claim 1 under 35 U.S.C. 103(a) is incorporated herein. (supra) In addition, the common state is an erased state (0 logic is expressed as the erased state).

15. As per claim 7, the rejection of claim 4 under 35 U.S.C. 103(a) is incorporated herein. (supra) In addition, step d is further defined by shifting the one bit not set to the common state one bit location toward a most significant bit (Mano, table 5-4; first state: Q3=0, Q2=0, Q1=0, Q0=1, next state: Q3=0, Q2=0, Q1=1, Q0=0).

16. As per claim 8, the rejection of claim 6 under 35 U.S.C. 103(a) is incorporated herein. (supra) In addition, the shifting of the one bit location is further defined by erasing the bits of the second non-volatile memory location and writing a new value such that the bits previously in the common state and remaining in a common state for the incremented value do not experience a write cycle (Mano, table 5-4; first state: Q3=0, Q2=0, Q1=0, Q0=1, next state: Q3=0, Q2=0, Q1=1, Q0=0; only Q1 experiences a full write cycle).

17. As per claim 9, the rejection of claim 1 under 35 U.S.C. 103(a) is incorporated herein. (supra) In addition, each multiple bit locations of the first and second non-volatile memory locations are independently controllable (Mano, fig. 5-8).

18. As per claim 10, the rejection of claim 1 under 35 U.S.C. 103(a) is incorporated herein. (supra) In addition, step c is further defined by translating the second value by way of a preset algorithm before combining the second value with the first value (the second value is least significant bits and the first value is the most significant bits).

19. As per claim 11, the rejection of claim 1 under 35 U.S.C. 103(a) is incorporated herein. (supra) In addition, the combining steps is further defined by the first value representing most significant bits and the second value representing a least significant bit such that the combination of the first and second values are a binary "OR" calculation (since the first value represents the most significant bits and the second value represents the least significant bits, the combination of the two values are consistent with operations including binary addition and binary "OR").

20. As per claim 12, the rejection of claim 1 under 35 U.S.C. 103(a) is incorporated herein. (supra) In addition, the total value is used to encrypt a transmission for a remote keyless entry system (Soenen, col. 1:25-35 and lines 60-67).

21. As per claim 13, the rejection of claim 1 under 35 U.S.C. 103(a) is incorporated herein. (supra) In addition, the first and second non-volatile memory locations are located within a transmitter of the remote keyless entry system, such that the first and second values provide for the storage of a rolling code (Soenen, col. 1:25-35 and lines 60-67; 20:5-24).

22. Claims 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Soenen in view of Mano.

23. As per claim 14, Soenen discloses a non-volatile memory device for use in a rolling code security system, wherein a 40-bit security code is incremented when a transmission button is depressed and this incremented 40-bit security code is stored in non-volatile memory. Soenen does not teach first and second memory devices for storing a total value used to form the coded signal, the first and second memory devices including multiple bit locations that represent first and second values, the first and second values combined to form the total value, and only one of the multiple bit locations completes a write cycle for each increment of the total value. However, counters are well-known in the art to provide such a feature: Mano discloses several counters, including a 4-bit binary counter, in which first and second memory devices (pg. 262, fig. 5-8; Q0,Q1 and Q2,Q3) include multiple bit locations that represent first and second values, the first and second values combined to form the total value, and only one of the multiple bit locations completes a write cycle for each increment of the total value (pg. 263, table 5-4). These counter designs are standard implementations of preserving incremented states as described in Soenen. Therefore, it would be obvious to one of ordinary skill in the art at the time the invention was made to combine the incrementing state preserving hardware of Mano and the rolling code security system of

Soenen, since counters are the basic elements to preserve incremented state (Mano, pg. 261, section 5-4). The aforementioned cover the limitations of claim 14.

24. As per claim 15, the rejection of claim 14 under 35 U.S.C. 103(a) is incorporated herein. (supra) In addition, the first non-volatile memory device includes the first value and the second non-volatile memory device includes the second value (by virtue of storing the two values).

25. As per claim 16, the rejection of claim 15 under 35 U.S.C. 103(a) is incorporated herein. (supra) In addition, a number of the multiple bit locations are disposed within the second non-volatile memory and the total value is incremented by shifting which of the multiple bit location disposed within the second non-volatile memory location are in a non-common state (Mano, pg. 264, table 5-5, when Q1 and Q0 are "11", and Q3 and Q2 are "00", the next state is "00" for Q1 and Q0, and "01" for Q3 and Q2).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Michaels USPN 5,420,925 discloses an encryption process for a rolling code system whereby a security code shift register includes a security code, which is updated by a first and second pseudo-random number generator.

Latka USPN 5,646,996 discloses storing rolling code values in an EEPROM for identification of a fob.

Communications Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jung W. Kim whose telephone number is 571-272-3804. The examiner can normally be reached on M-F 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gilberto Barron can be reached on 571-272-3799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jung W Kim
Examiner
Art Unit 2132

August 30, 2005

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